

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1669	703/2.ccls. and @ad<"20031011"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/14 08:18
L2	388	703/2.ccls. and @ad>"20031010"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/14 08:33

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	54	vhdl-ams	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/14 08:41
L6	96	((mixed adj signal) or mixed-signal) and (finite adj state) and @ad<"20031212"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/14 08:49

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[C Toumazou](#)

[J Hughes](#)

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[E Christen](#)

[A Inc](#)

[BOOK] **Switched-Currents: An Analogue Technique for Digital Technology**

C Toumazou, JB Hughes - 1993 - books.google.com

... Volume 2 **Analogue** IC design: the current-mode approach C. Toumazou, FJ Lidgey and

DG Haigh (Editors) Volume 3 **Analogue-digital** ASICs RS Soin, F. Maloberti and J ...

[Cited by 187](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

A real time digital simulator for testing relays - group of 2 »

PG McLaren, R Kuffel, R Wierckx, J Giesbrecht, L ... - Power Delivery, IEEE Transactions on, 1992 - [ieeexplore.ieee.org](#)

... simulators use scaled down models of system elements, a **digital simulator** models these ... should be compared to the extent of an **analogue** TNA to ... h user **interface** ...

[Cited by 52](#) - [Related Articles](#) - [Web Search](#)

A simple digital fading simulator for mobile radio - group of 2 »

E Casas, C Leung - Vehicular Technology, IEEE Transactions on, 1990 - [ieeexplore.ieee.org](#)

... when used with the mixer **interface** circuit described ... ital signal noise coupling onto the **analog** circuitry and D ... The **digital** and **analog** circuits used sep- arate ...

[Cited by 25](#) - [Related Articles](#) - [Web Search](#)

Simulation techniques for mixed analog/digital circuits - group of 2 »

EL Acuna, JP Dervenis, AJ Pagones, FL Yang, RA ... - Solid-State Circuits, IEEE Journal of, 1990 - [ieeexplore.ieee.org](#)

... iSPLICE3 for the analysis of mixed **analog/digital** circuits ... hierarchical schematic capture package called iSPI (**Simulation Program Interface**) for design ...

[Cited by 18](#) - [Related Articles](#) - [Web Search](#)

On a new generation of torque controlled light-weight robots - group of 4 »

G Hirzinger, A Albu-Schaffer, M Hahnle, I Schaefer ... - PROC IEEE INT CONF ROB AUTOM, 2001 - [robotic.de](#)

... **analog digital** (processor) **digital** (FPGA) Speed ++ o + Flexibility - ++ + **Simulation**

Tools ... [Table 2] The AD-**interface**, the DSP-**interface** (dual port ram ...

[Cited by 47](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

VHDL-AMS-a hardware description language for analog andmixed-signal applications - group of 2 »

E Christen, K Bakalar, A Inc, OR Beaverton - ... and Systems II: **Analog** and **Digital** Signal Processing, IEEE ..., 1999 - [ieeexplore.ieee.org](#)

... **interface** quantity with mode in, input, and one **interface** quantity with ... IEEE

TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: **ANALOG** AND **DIGITAL** SIGNAL PROCESSING ...

[Cited by 91](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

... logic controller for DC/DC converters: design, computer simulation, and experimental evaluation - group of 4 »

WC So, CK Tse, YS Lee - Power Electronics, IEEE Transactions on, 1996 - [ieeexplore.ieee.org](#)

... Logic Controller for DC/DC Converters: Design, Computer **Simulation**, and Experimental ...

Traditional frequency- domain **analog** methods are predominantly used in ...

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All Verilog mixed-signal simulator with analog behavioral and noisemodels - group of 2 »

MK Mayes, SW Chin - **Analog** and Mixed IC Design, 1996., IEEE-CAS Region 8 ..., 1996 - [ieeexplore.ieee.org](#)

... 2] contains 60 signals at the partition **interface** (see fig. ... The 32-bit micro-controller calibrates the **analog** circuitry and performs **digital** correction.The ...

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1.   **Crosstalk effects in mixed-signal ICs in deep submicron digital CMOS technology • ARTICLE**
Microelectronics Journal, Volume 31, Issues 11-12, December 2000, Pages 893-904
V. Liberali, R. Rossi and G. Torelli
[SummaryPlus](#) | [Full Text + Links](#) | [PDF \(471 K\)](#)

2.   **A generic interface chip for capacitive sensors in low-power multi-parameter microsystems • ARTICLE**
Sensors and Actuators A: Physical, Volume 84, Issue 3, 1 September 2000, Pages 351-361
Navid Yazdi, Andrew Mason, Khalil Najafi and Kensall D. Wise
[SummaryPlus](#) | [Full Text + Links](#) | [PDF \(3499 K\)](#)

3.   **CMOS technology for mixed signal ICs • ARTICLE**
Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 395, Issue 3, 21 August 1997, Pages 298-305
Marcel J. M. Pelgrom and Maarten Vertregt
[Abstract](#) | [Abstract + References](#) | [PDF \(769 K\)](#)

4.   **CMOS technology for mixed signal ICs • ARTICLE**
Solid-State Electronics, Volume 41, Issue 7, July 1997, Pages 967-974
M. J. M. Pelgrom and M. Vertregt
[Abstract](#) | [Abstract + References](#) | [PDF \(804 K\)](#)

5.   **Design tools for oversampled data converters: Needs and solutions • ARTICLE**
Microelectronics Journal, Volume 23, Issue 8, December 1992, Pages 641-650
V. F. DiasV. Liberali and F. Maloberti
[Abstract](#)

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1.   **IPRAIL—intellectual property reuse-based analog IC layout automation • ARTICLE**
Integration, the VLSI Journal, Volume 36, Issue 4, November 2003, Pages 237-262
Nuttorn Jangkrajarn, Sambuddha Bhattacharya, Roy Hartono and C. -J. Richard Shi
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2.   **Analog and mixed signal test techniques for SoCs • EDITORIAL**
Microelectronics Journal, Volume 34, Issue 10, October 2003, Pages 887-888
Hans G. Kerkhoff and Bozena Kaminska
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3.   **Behavioral test generation modeling approach for mixed-signal IC verification • ARTICLE**
Microelectronics Journal, Volume 34, Issue 10, October 2003, Pages 907-912
Veikko Loukusa
[SummaryPlus](#) | [Full Text + Links](#) | [PDF \(284 K\)](#)

4.   **Multi-level hierarchical analogue fault simulation • ARTICLE**
Microelectronics Journal, Volume 33, Issue 10, October 2002, Pages 815-821
Bernd Straube, Wolfgang Vermeiren and Volker Spenke
[SummaryPlus](#) | [Full Text + Links](#) | [PDF \(734 K\)](#)

5.   **A high-performance VHDL-based virtual tester: a concept and a solution • SHORT COMMUNICATION**
Microelectronics Journal, Volume 33, Issue 10, October 2002, Pages 855-859
Gunter Kramp and Marco Rona
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6.   **System level simulation of a double stator wobble electrostatic micromotor • ARTICLE**
Sensors and Actuators A: Physical, Volume 99, Issue 3, 5 June 2002, Pages 312-320
Aitor Endemaño, Marc P. Y. Desmulliez and Matthew Dunnigan
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7.   **Microsensor clusters • ARTICLE**
Microelectronics Journal, Volume 33, Issues 1-2, 2 January 2002, Pages 107-119

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Results for "(digital analog interface) <and> (pyr >= 1951 <and> pyr <= 2003)"

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- ☐ **Fuzzy-logic digital-analogue interfaces for accurate mixed-signal simulation**
 Kazmierski, T.J.;
Design, Automation and Test in Europe, 1998...Proceedings
 23-26 Feb. 1998 Page(s):941 - 944
 Digital Object Identifier 10.1109/DATE.1998.655980
[AbstractPlus](#) | Full Text: [PDF](#)(28 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **ESD protection to overcome internal gate oxide damage on digital-analog interface of mixed-mode CMOS IC's**
 Ming-Dou Ker; Ta-Lee Yu;
Reliability of Electron Devices, Failure Physics and Analysis, 1996. Proceedings of the 7th European Symposium on
 8-11 October 1996 Page(s):1727 - 1730
[AbstractPlus](#) | Full Text: [PDF](#)(236 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **Implementation trade-offs for a short-headway vehicle-follower automated transit system**
 Pue, A.J.;
Vehicular Technology, IEEE Transactions on
 Volume 28, Issue 1, Feb 1979 Page(s):46 - 55
[AbstractPlus](#) | Full Text: [PDF](#)(792 KB) IEEE JNL
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- ☐ **Realization of an adaptive delta modulation codec robust to channel errors**
 Moriya, T.; Murano, K.; Matsuda, K.;
Circuits and Systems, IEEE Transactions on
 Volume 25, Issue 7, Jul 1978 Page(s):476 - 481
[AbstractPlus](#) | Full Text: [PDF](#)(832 KB) IEEE JNL
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- ☐ **Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI**
 Ming-Dou Ker;
Electron Devices, IEEE Transactions on
 Volume 46, Issue 1, Jan. 1999 Page(s):173 - 183
 Digital Object Identifier 10.1109/16.737457
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1008 KB) IEEE JNL
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- ☐ **Point-to-point connectivity between neuromorphic chips using address events**
 Boahen, K.A.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]
 Volume 47, Issue 5, May 2000 Page(s):416 - 434
 Digital Object Identifier 10.1109/82.842110

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- ☐ 1. **Power semiconductor device modeling with Model Architect**
Mantooth, H.A.; Skudlarek, J.P.; Carlson, J.R.; Cooper, D.K.; Getreu, I.E.; Graham, G.; Pothier, S.; Vedam, R.; Wolff, C.M.;
[Computers in Power Electronics, 2000. COMPEL 2000. The 7th Workshop on](#)
16-18 July 2000 Page(s):3 - 9
Digital Object Identifier 10.1109/CIPE.2000.904683
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- ☐ 2. **The ALTRO chip: a 16-channel A/D converter and digital processor for gas detectors**
Bosch, R.E.; de Parga, A.J.; Mota, B.; Musa, L.;
[Nuclear Science, IEEE Transactions on](#)
Volume 50, Issue 6, Part 2, Dec. 2003 Page(s):2460 - 2469
Digital Object Identifier 10.1109/TNS.2003.820629
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- ☐ 3. **Design considerations for minimal-power wireless spread spectrum circuits and systems**
Myers, B.A.; Willingham, J.B.; Landy, P.; Webster, M.A.; Frogge, P.; Fischer, M.;
[Proceedings of the IEEE](#)
Volume 88, Issue 10, Oct. 2000 Page(s):1598 - 1612
Digital Object Identifier 10.1109/5.888998
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- ☐ 4. **An all-digital built-in self-test for high-speed phase-locked loops**
Seongwon Kim; Soma, M.;
[Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on \[see also Circuits and Systems II: Express Briefs, IEEE Transactions on\]](#)
Volume 48, Issue 2, Feb. 2001 Page(s):141 - 150
Digital Object Identifier 10.1109/82.917782
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(160 KB\)](#) | IEEE JNL
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- ☐ 5. **Quick start crystal oscillator circuit**
Blanchard, S.A.;
[University/Government/Industry Microelectronics Symposium, 2003. Proceedings of the 15th Biennial](#)
30 June-2 July 2003 Page(s):78 - 81
[AbstractPlus](#) | [Full Text: PDF\(349 KB\)](#) | IEEE CNF
[Rights and Permissions](#)
- ☐ 6. **Mixed signal decoder for audio frequency applications**
Hamed, H.M.; Zaguoul, M.E.; Salama, A.; Talkhan, E.A.;
[Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on](#)

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IEEE CNF IEEE Conference Proceeding

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- ☐ 1. **Microstrip antennas on synthesized low dielectric-constant substrates**
Gauthier, G.P.; Courtay, A.; Rebeiz, G.M.;
[Antennas and Propagation, IEEE Transactions on](#)
Volume 45, Issue 8, Aug. 1997 Page(s):1310 - 1314
Digital Object Identifier 10.1109/8.611252
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(152 KB) IEEE JNL
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- ☐ 2. **An improved behavioral IGBT model and its characterization tool**
Min Zhang; Courtay, A.; Zhilian Yang;
[Electron Devices Meeting, 2000. Proceedings. 2000 IEEE Hong Kong](#)
24 June 2000 Page(s):142 - 145
Digital Object Identifier 10.1109/HKEDM.2000.904235
[AbstractPlus](#) | Full Text: [PDF](#)(376 KB) IEEE CNF
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- ☐ 3. **Microstrip antennas on localized micromachined dielectric substrates**
Courtay, A.; Gauthier, G.P.; Rebeiz, G.M.;
[Antennas and Propagation Society International Symposium, 1996. AP-S. Digest](#)
Volume 2, 21-26 July 1996 Page(s):1246 - 1249 vol.2
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VHDL-AMS-a hardware description language for **analog** and mixed-signal applications - group of 2 »

E Christen, K Bakalar, A Inc, OR Beaverton - ... and Systems II: **Analog** and **Digital** Signal Processing, IEEE ... , 1999 - [ieeexplore.ieee.org](#)

... 10, OCTOBER 1999 Fig. 6. **VHDL-AMS** model of a comparator with hysteresis. ... It is instructive to reconstruct the **state** transition **diagram** of this model ...

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[book] **The System Designer's Guide to VHDL-AMS: Analog, Mixed-Signal, and Mixed-Technology Modeling**

PJ Ashenden, GD Peterson, DA Teegarden - 2002 - [books.google.com](#)

... Preface **VHDL-AMS** is a language for describing **digital**, **analog** and mixed-signal systems. It is an extension of the **digital** hardware description language V ...

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Analog and Mixed-Signal Modeling Using the **VHDL-AMS** Language - group of 26 »

E Christen, K Bakalar, AM Dewey, E Moser - 36th ACM/IEEE Design and Automation Conference, 1999 - [tams-www.informatik.uni-hamburg.de](#)

... 968 ((ÄWC9G 6HTÄU□□□□vhy **VHDL-AMS** Highlights (2) ... Signal-flow descriptions • Mixed-signal interfaces Models can have **digital** and **analog** ports ...

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SystemC-AMS requirements, design objectives and rationale - group of 15 »

A Vachoux, C Grimm, K Einwich - Design, Automation and Test in Europe Conference and ... , 2003 - [ieeexplore.ieee.org](#)

... Figure 1. Simplified block **diagram** of a subscriber ... in the definition of the **VHDL-AMS** hardware description ... like a transfer function or **state**-space description. ...

Cited by 14 - [Related Articles](#) - [Web Search](#)

Co-simulation of Embedded Electronic Systems

M Oyamada, FR Wagner - 12 ndEuropean Simulation Symposium. Hamburgo, Alemanha, Out, 2000 - [caracol.inf.ufrgs.br](#)

... used for modeling **digital** hardware, **VHDL-AMS** may be ... editor implements extensions to **diagrams** usually proposed ... discrete computation of the **state**-variable method ...

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Bluetooth transceiver design and simulation with **VHDL-AMS** - group of 2 »

M Sida, R Ahola, D Wallner, M Graphics, G Munich - Circuits and Devices Magazine, IEEE, 2003 - [ieeexplore.ieee.org](#)

... 2. Block **diagram** of the BlueTraC radio transceiver ... simulated the complete transceiver using **VHDL-AMS** and ADMS ... down sequences as well as the **state** machine con ...

Cited by 6 - [Related Articles](#) - [Web Search](#)

Design of mixed-signal systems-on-a-chip - group of 10 »

K Kundert, H Chang, D Jefferies, G Lamant, E ... - Computer-Aided Design of Integrated Circuits and Systems, ... , 2000 - [ieeexplore.ieee.org](#)

... is to use Verilog-AMS or **VHDL-AMS** for both ... The block-**diagram** used in the simulation of the ... distribution is significantly different when **analog** and **digital** ...

Cited by 48 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Behavioral Partitioning in the Synthesis of Mixed Analog-Digital Systems - group of 13 »

S Ganesan, R Vemuri - Proc. Design Automation Conference, 2001 - [doi.ieeeecomputersociety.org](#)

... **State** space models of the same are generated, and then converted into block **diagrams**. ... flow graph representation, ABLOX from **VHDL-AMS** specifications. ...

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[M Bushnell](#)

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VHDL-AMS-a hardware description language for analog and mixed-signal applications - group of 2 »

E Christen, K Bakalar, A Inc, OR Beaverton - Circuits and Systems II: **Analog and Digital Signal** ..., 1999 - [ieeexplore.ieee.org](#)

... are interpreted correctly, while providing for an efficient **simulation**. ... a hardware description language for **analog, digital, and mixed-signal** applications. ...

Cited by 91 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Design for testability of mixed signal integrated circuits

KD Wagner, TW Williams - Test Conference, 1988. Proceedings. 'New Frontiers in Testing' ..., 1988 - [ieeexplore.ieee.org](#)

... **Digital** and **analog** circuitry must be isolated from each other, ie, an un- controlled **analog signal** must not be able ... Any **mixed-mode** chip **simulation** [11] of ...

Cited by 53 - [Related Articles](#) - [Web Search](#)

Computer-aided design of analog and mixed-signal integrated circuits - group of 2 »

GGE Gielen, RA Rutenbar - Proceedings of the IEEE, 2000 - [ieeexplore.ieee.org](#)

... like **analog simulator** to an efficient **digital simulator**. These so-called glued **mixed-mode** simulators ... between **analog** and **digital signal** representations and of ...

Cited by 124 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[book] Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal Vlsi Circuits

MJ Bushnell, VD Agrawal - 2000 - [books.google.com](#)

... 380 10.9 Summary 382 I 1 MODEL-BASED **ANALOG AND MIXED-SIGNAL TEST** 385 ... 395 11.5.4 Monte-Carlo **Simulation** 397 ... 398 11.6.2 ATPG Using **Signal** Flow Graphs 406 ...

Cited by 355 - [Related Articles](#) - [Web Search](#) - [Library Search](#)

Synthesis Tools for Mixed-Signal ICs: Progress on Frontend and Backend Strategies - group of 8 »

LR Carley, G Gielen, RA Rutenbar, W Sansen - Proc. DAC, 1996 - [doi.ieeeecomputersociety.org](#)

... Given the success of synthesis and semi-custom layout in **digital** designs, we focus our ... And, we do not cover **analog** and **mixed-signal simulation** strategies. ...

Cited by 55 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

All Verilog mixed-signal simulator with analog behavioral and noise models - group of 2 »

MK Mayes, SW Chin - **Analog and Mixed IC Design**, 1996., IEEE-CAS Region 8 ..., 1996 - [ieeexplore.ieee.org](#)

... All **Digital Simulation** Typical **mixed-signal simulation** techniques use separate **analog** and **digital** simulators linked through a threshold function at the ...

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[book] Synthesis and Optimization of Digital Circuits - group of 5 »

G De Micheli - 1994 - McGraw-Hill Higher Education

... Map to Methodologies for **Mixed-Signal System Design** & ... on Modeling and Computer **Simulation** (TOMACS), v ... Multiprocessors, Journal of VLSI **Signal Processing Systems** ...

Cited by 914 - [Related Articles](#) - [Web Search](#) - [Library Search](#)

Design of mixed-signal systems-on-a-chip - group of 10 »

K Kundert, H Chang, D Jefferies, G Lamant, E ... - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 - [ieeexplore.ieee.org](#)

... While not necessarily implementing the **analog** portions, this ... description languages used for **simulation**, such as ... to drive block placement in **mixed signal** systems ...

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HYPER: an interactive synthesis environment for high performance real time applications

CM Chu, M Potkonjak, M Thaler, J Rabaey - Computer Design: VLSI in Computers and Processors, 1989.
1989 - [ieeexplore.ieee.org](#)

... L2. Related Work Until now, synthesis systems for Digital **Signal** Processing (DSP) have focused either on control oriented architectures (such as CATHEDRAL-II ...
Cited by 40 - [Related Articles](#) - [Web Search](#)

VHDL-AMS-a hardware description language for analog and mixed-signal applications - group of 2 »

E Christen, K Bakalar, A Inc, OR Beaverton - ... II: Analog and Digital **Signal** Processing, IEEE Transactions ...
1999 - [ieeexplore.ieee.org](#)

... output **signal** when entering the state, defining the condition when the **finite state machine** leaves the ... [4] Definition of Analog and **Mixed Signal** Extensions to ...
Cited by 91 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Hierarchical finite state machines with multiple concurrency models - group of 13 »

A Girault, B Lee, EA Lee - Computer-Aided Design of Integrated Circuits and Systems, ..., 1999 - [ieeexplore.ieee.org](#)

... The block diagram languages used in **signal** processing, for example, almost ... process networks with FSM's [4]. The codesign **finite state machine** (CFSM) model [16 ...
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... then, the computational complexity of a **cubic** substrate model ... 33.9 dB (for full 10×

logic **transitions** as shown ... The **simulation** times for the various cases was ...

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... The result is the J state **transition** functions @V(O ... In order to coordinate the

simulation of these ... a behavioral linear amplifier with a **cubic** function which ...

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... Each **simulation** was initiated with a run performed using ... the system is found to remain

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